

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) Martin Vorbach et al.	
	Filing Date March 1, 2005	Group Art Unit 2193

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	90/010,979	May 4, 2010 (filing date)	Vorbach et al.			
	90/011,087	July 8, 2010 (filing date)	Vorbach et al.			
	4,623,997	November 18, 1986	Tulpule			
	5,212,777	May 18, 1993	Gove et al.			
	5,572,710	November 5, 1996	Asano et al.			
	5,606,698	February 25, 1997	Powell			
	5,627,992	May 6, 1997	Baror			
	5,659,785	August 19, 1997	Pechanek et al.			
	5,696,791	December 9, 1997	Yeung			
	5,804,986	September 8, 1998	Jones			
	6,049,866	April 11, 2000	Earl			
	6,298,396	October 2, 2001	Loyer et al.			
	6,434,672	August 13, 2002	Gaither			
	6,512,804	January 28, 2003	Johnson et al.			
	6,553,479	April 22, 2003	Mirsky et al.			
	6,598,128	July 22, 2003	Yoshioka et al.			
	6,606,704	August 12, 2003	Adiletta et al.			
	6,745,317	June 1, 2004	Mirsky et al.			
	6,751,722	June 15, 2004	Mirsky et al.			
	6,975,138	December 13, 2005	Pani et al.			
	7,028,107	April 11, 2006	Vorbach et al.			
	7,382,156	June 3, 2008	Pani et al.			
	2002/0156962	October 24, 2002	Chopra et al.			
	2004/0039880	February 26, 2004	Pentkovski et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	7-182167	July 21, 1995	Japan			Abstract	
	7-182160	July 21, 1995	Japan			Abstract	
	8-106443	April 23, 1996	Japan			Abstract	
	9-237284	September 9, 1997	Japan			Abstract	
	11-046187	February 16, 1999	Japan			Abstract	
	2001-236221	August 31, 2001	Japan			Abstract	
	2001-510650	July 31, 2001	Japan			Abstract only	
	2002-0033457	January 31, 2002	Japan			Abstract	
	3-961028	August 15, 2007	Japan			Abstract	

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**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "2. TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices," Altera Corporation, July 2005, 28 pages.
	Altera, "APEX II Programmable Logic Device Family," Altera Corporation Data Sheet, August 2002, Ver. 3.0, 99 pages.
	Becker, J., "A Partitioning Compiler for Computers with Xputer-based Accelerators," 1997, Kaiserslautern University, 326 pp.
	"BlueGene/L – Hardware Architecture Overview," BlueGene/L design team, IBM Research, October 17, 2003 slide presentation, pp. 1-23.
	"BlueGene/L: the next generation of scalable supercomputer," Kissel et al., Lawrence Livermore National Laboratory, Livermore, California, November 18, 2002, 29 pages.
	BlueGene Project Update, January 2002, IBM slide presentation, 20 pages.
	BlueGene/L, "An Overview of the BlueGene/L Supercomputer," The BlueGene/L Team, IBM and Lawrence Livermore National Laboratory, 2002 IEEE, pp. 1-22.
	Epstein, Dave, "IBM Extends DSP Performance with Mfxt," Microprocessor Report, Vol. 9, No. 16 (MicroDesign Resources), December 4, 1995, pp. 1-4 [XL0029013].
	Galanis, M.D. et al., "Accelerating Applications by Mapping Critical Kernels on Coarse-Grain Reconfigurable Hardware in Hybrid Systems," Proceedings of the 13 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2005, 2 pages.
	Guo, Z. et al., "A Compiler Intermediate Representation for Reconfigurable Fabrics," University of California, Riverside, Dept. of Electrical Engineering, IEEE 2006, 4 pages.
	Gwennap, Linley, "P6 Underscores Intel's Lead," Microprocessor Report, Vol. 9., No. 2, February 16, 1995 (MicroDesign Resources), p. 1 and pp. 6-15.
	Gwennap, Linley, "Intel's P6 Bus Designed for Multiprocessing," Microprocessor Report, Vol. 9, No. 7 (MicroDesign Resources), May 30, 1995, p.1 and pp. 6-10.
	Hartenstein et al., "Parallelizing Compilation for a Novel Data-Parallel Architecture," 1995, PCAT-94, Parallel Computing: Technology and Practice, 13 pp.
	Hartenstein et al., "A Two-Level Co-Design Framework for Xputer-based Data-driven Reconfigurable Accelerators," 1997, Proceedings of the Thirtieth Annual Hawaii International Conference on System Sciences, 10 pp.
	Hauser, John Reid, (Dissertation) "Augmenting A Microprocessor with Reconfigurable Hardware," University of California, Berkeley, Fall 2000, 255 pages. (submitted in 3 PDFs, Parts 1-3)
	Hauser, John R., "The Garp Architecture," University of California at Berkeley, Computer Science Division, October 1997, pp. 1-55.
	Huang, Libo et al., "A New Architecture for Multiple-Precision Floating-Point Multiply-Add Fused Unit Design," School of Computer National University of Defense Technology, China, IEEE 2007, 8 pages.
	IMEC, "ADRES multimedia processor & 3MF multimedia platform," Transferable IP, IMEC Technology Description, (Applicants believe the date to be October 2005), 3 pages.
	Intel, "Pentium Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide," Intel Corporation, December 1995, [submitted in 4 PDF files: Part I, Part II, Part III and Part IV], 458 pages.
	Jo, Manhwee et al., "Implementation of Floating-Point Operations for 3D Graphics on a Coarse-Grained Reconfigurable Architecture," Design Automation Laboratory, School of EE/CS, Seoul National University, Korea, IEEE 2007, pp. 127-130.
	Venkatachalam et al., "A highly flexible, distributed multiprocessor architecture for network processing," Computer Networks, The International Journal of Computer and Telecommunications Networking, Vol. 41, No. 5, April 5, 2003, pp. 563-568.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	XILINX, White Paper 370: (Virtex-6 and Spartan-6 FPGA Families) "Reducing Switching Power with Intelligent Clock Gating," Frederic Rivoallon, May 3, 2010, pp. 1-5.
	XILINX, White Paper 298: (Spartan-6 and Virtex-6 Devices) "Power Consumption at 40 and 50 nm," Matt Klein, April 13, 2009, pp. 1-21.
	Xilinx, Inc.'s and Avnet, Inc.'s Disclosure Pursuant to P.R. 4-2; <i>PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.</i> , Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, 4 pages.
	Xilinx, Inc.'s and Avnet, Inc.'s Disclosure Pursuant to P.R. 4-1; <i>PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.</i> , Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, 9 pages.

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EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Defendant's Claim Construction Chart for P.R. 4-2 Constructions and Extrinsic Evidence for Terms Proposed by Defendants, <i>PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.</i> , Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-19.
	PACT's P.R. 4-1 List of Claim Terms for Construction, <i>PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.</i> , Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-7.
	PACT's P.R. 4-2 Preliminary Claim Constructions and Extrinsic Evidence, <i>PACT XPP TECHNOLOGIES, AG. V. XILINX, INC. and AVNET, INC.</i> , Case No. 2:07-cv-00563-TJW-CE, U.S. District Court for the Eastern District of Texas, Dec. 28, 2007, pp. 1-16, and EXHIBITS re EXTRINSIC EVIDENCE Parts in seven (7) separate additional PDF files (Parts 1-7).
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	